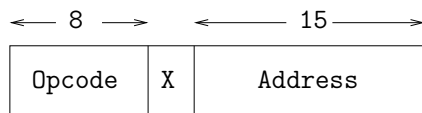


SIC and SIC/XE Architectures

Ref: Chapter 1 and Appendix A of [Beck].

Details regarding SIC:

- Allows only integers and characters.
- Memory size = 2^{15} bytes. (Byte address: 15 bits).
- Word size = 3 bytes (or 24 bits).
- Characters: 1 byte (ASCII).
- Integers use 3 bytes; 2's complement for negative values.
- Five registers (denoted by A, X, L, PC and SW).
- Instruction format:



Note: X is the “index bit”.

Instruction set of SIC:

Ref: Appendix A of [Beck].

(a) Examples of Load/Store Instructions:

LDA m
STA m
STX m

(b) Examples of Arithmetic Instructions:

Note: Here, register A is always an operand. Also, the result is in A.

ADD m
DIV m

(c) Comparison Instruction:

COMP m

Note: Compares the contents of A with the contents of the specified memory location; sets CC to indicate >, = or <.

(d) Conditional Jump Instructions:

JLT	m
JEQ	m
JGT	m

(e) Procedure call/return Instructions:

JSUB	m
RSUB	

(f) I/O Instructions:

RD	d
WD	d
TD	d

Notes:

- Each I/O device has an 8-bit ID.
- I/O done one byte at a time.

Outline for I/O in SIC:

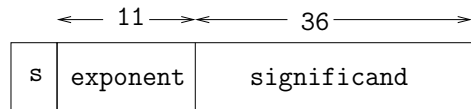
1. repeat
 Test device
 until device is ready.
2. Read/write one byte.

Note: This method of I/O is called “Busy-Wait” or “Programmed” I/O.

Details regarding SIC/XE:

- Allows integers, characters and floating point values.
- Memory size = 2^{20} bytes. (Byte address: 20 bits).
- Word size = 3 bytes (or 24 bits).
- Four additional registers (denoted by B, S, T and F).

Floating point format:

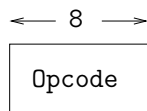


Note: The 11-bit exponent is stored in Biased-1024 form.

Instruction Formats for SIC/XE:

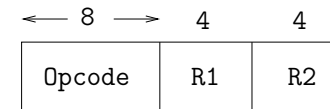
- Addresses must be 20 bits long.
- Uses both relative addressing and extended addressing.
- Instructions may be 1, 2, 3 or 4 bytes long.

1-Byte format:



Example: FLOAT

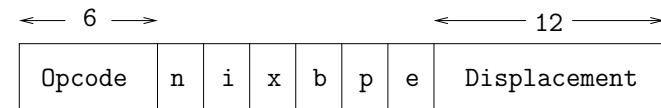
2-Byte format:



Examples:

RMO S, T
MULR S, T

3-Byte format:

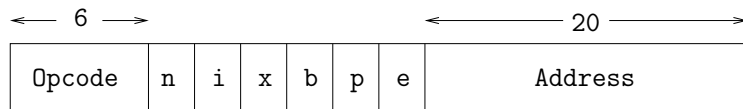


Notes:

- x – index bit (as before).
- Bits b and p specify **relative** addressing.
 - (1) b = 1 and p = 0: Relative to B.
 - (2) b = 0 and p = 1: Relative to PC.
 - (3) b = 0 and p = 0: Direct address.

- In B-relative mode, displacement is treated as an unsigned integer.
- In PC-relative mode, displacement is treated as an integer in 2's complement form.
- Bits i and n specify extended addressing modes.
 - (1) $i = 1$ and $n = 0$: **Immediate** mode.
 - (2) $i = 0$ and $n = 1$: **Indirect** mode.
 - (3) $(i = n)$: **Simple** addressing.
- Bit e is always zero for 3-byte instructions.

4-Byte format:



Notes:

- Bits b and p are always 0.
- Bits e is always 1.

SIC/XE Instruction Set:

- Includes all SIC instructions.
- New instructions (e.g. LDB, STB).
- Floating point instructions (e.g. ADDF, MULF).
- Register-to-register instructions (e.g. ADDR, MULR).

Examples of address calculation:

- To be presented in class.

SIC Assembly Language:

- Simple program examples in Handout 1.1.

Some known architectures:

- Brief discussion on MIPS, Pentium and SPARC.
- Others from [Beck] left as reading assignment.

MIPS Architecture (Review):

- Commonly used in SGI workstations.
- Load/store architecture; number of instructions is around 100 (RISC).
- Memory address = 32 bits; word size = 32 bits; processor can support both big endian and little endian ordering.
- Instruction length = 32 bits.
- Separate co-processors C0 (for exception handling) and C1 (floating point operations).
- 32 CPU registers for integer operations; each register is 32 bits long.
- 32-bit (single precision) and 64-bit (double precision) floating point registers are available; floating point representation based on IEEE FPS.
- Simple addressing modes (immediate and base + displacement); load address instruction to support indirect addressing.

- Supports all basic data types of C (int, char, float and double).

IA-32 Architecture (Intel):

- Started with Intel 80386 and has continued up to Pentium 4.
- Memory address = 32 bits; little endian; word size = 32 bits.
- 8 general purpose 32-bit registers (R0 through R7) and 8 floating point 64-bit registers (FP0 through FP7).
- Instruction Pointer (PC) and Status Register (containing condition code).
- More than 400 instructions; instruction lengths vary from 1 to 12 bytes (CISC).
- A variety of addressing modes (e.g. immediate, direct, register, register indirect, base + displacement, base + index, etc).

- Supports all basic data types of C (int, char, float and double). Also supports quad precision for floating point.
- Separate floating point processor.

Sun SPARC Architecture:

- Used in Sun workstations. (Designed in 1987 and has evolved to SuperSPARC, UltraSPARC and UltraSPARC-II.)
- Load/store architecture; Number of instructions is around 100 (RISC).
- Memory address = 64 bits; big endian; word size = 32 bits.
- Instruction length = 32 bits.
- 64-bit registers for integer operations.
- Has a “register file” consisting of 64 to 512 registers. Each procedure can use only a “window” of 32 registers.

- Windows of different procedures may overlap (to support parameter passing).
- Register file of floating point registers.
- Each floating point register is 32 bits long to provide for single precision IEEE FPS; registers are paired to support double precision.
- Fewer addressing modes compared to IA-32 (e.g. immediate, register indirect + displacement, register indirect + index, etc).
- Supports all basic data types of C (int, char, float and double).
- Separate floating point processor.